In The Claims

1. Cancelled

2. Cancelled

3. Cancelled

4. (Currently Amended) The active pixel sensor circuit of Claim ~~1~~ 19, wherein a charge from the photodetector is transferred to a gate capacitance of the driver transistor via the snapshot transistor.

5. (Original) The active pixel sensor circuit of Claim 4, wherein the reset transistor discharges any charge left on the photodetector along with any charge on the gate of the driver transistor during a reset operation.

6. (Original) The active pixel sensor circuit of Claim 5, wherein the reset transistor is disabled during a signal integration mode and a snapshot image capture mode.

7. (Original) The active pixel sensor circuit of Claim 6, wherein, after snapshot image capture, the reset transistor is enabled in order to drain any unwanted charge that is generated after the integration mode.

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18. Cancelled

19. (Previously Presented) An active pixel sensor circuit comprising:

a photodetector;

a reset transistor connected between the photodetector and a first bus;

a snapshot transistor having a node connected to the photodetector;

a driver transistor connected to a row driver bus and the snapshot transistor;

a row driver circuit connected to the row driver bus;

an isolation transistor connected between the driver transistor and a column bus; and

a column buffer connected to the column bus;

wherein the transistors are MOSFETs and a tapered reset signal is applied to the reset transistor in order to reset the photodetector, and wherein during a reset operation, the row driver circuit grounds the driver transistor such that at least a portion of the column buffer acts as a current source for a feedback amplifier formed by the driver transistor, isolation transistor, and the column buffer.

20. (Previously Presented) A CMOS imager array circuit comprising:

a photodetector;

a reset MOSFET having a source connected to the photodetector, a gate connected to a reset input signal, and a drain connected to a first bus;

a snapshot MOSFET having a source connected to the photodetector and a gate connected to a snapshot signal;

a driver MOSFET having a drain connected to a row driver bus and a gate connected to a drain of the snapshot MOSFET;

a row driver circuit connected to the row driver bus;

an isolation MOSFET having a drain connected to a source of the driver MOSFET, a gate connected to an access signal, and a source connected to a column bus; and

a column buffer connected to the column bus;

wherein a tapered reset signal is applied to the reset MOSFET in order to reset the photodetector, and wherein during a reset operation, the row driver circuit grounds the driver transistor such that at least a portion of the column buffer acts as a current source for a feedback amplifier formed by the driver transistor, isolation transistor, and the column buffer.

21. (Previously Presented) The CMOS imager array circuit of Claim 20, wherein the row driver circuit and the column buffer are shared among a plurality of pixel circuits.

22. (New) The imager array of Claim 21, wherein the reset, snapshot, driver and isolation MOSFETs are all of the same polarity.

23. (New) The CMOS imager array of Claim 22, wherein a charge from the photodetector is transferred to a gate capacitance of the driver MOSFET via the snapshot MOSFET.

24. (New) The CMOS imager array of Claim 23, wherein the reset MOSFET discharges any charge left on the photodetector along with any charge on the gate of the driver MOSFET during a reset operation.

25. (New) The CMOS imager array of Claim 24, wherein the reset MOSFET is disabled during a signal integration mode and a snapshot image capture mode.

26. (New) The CMOS imager array of Claim 25, wherein, after snapshot image capture, the reset MOSFET is enabled in order to drain any unwanted charge that is generated after the integration mode.